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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,826	12/27/2001	Kazunobu Toguchi	US 010721	5494

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,826	TOGUCHI ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☒ Claim(s) 7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 March 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 4, 5, 6, 7, 8, 9, 11, 13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,728,809 to Suzuki et al. ("Suzuki").

3. In reference to Claim 1, Suzuki teaches (a) implementing a register table by a portal that contains a plurality of entries for storing respective remote delay values, which are equivalent to timeout values, from a local bus of a portal to a particular destination bus in a same net, wherein an Nth entry of the register table is corresponding to a bus ID of N (See Figure 1 Numbers 112 and 300 and Column 5 Lines 11-44); (b) intercepting a delay response message en route to a particular-addressed node by an exit portal if the delay response message is addressed to the

local bus of the portal, the delay response message comprising remote timeout values (See Column 4 Line 65 – Column 5 Line 10); (c) storing the remote delay values contained in the delay response message intercepted in step (b) in a corresponding entry of the plurality of entries in the register table implemented in step (a) (See Column 5 Lines 11-44); (d) forwarding the delay response message intercepted in step (b) to the particular-addressed node (See Column 4 Line 53 – Column 5 Line 10); (e) intercepting by a portal of a delay request message from an initial requester, if the remote delay values from the local bus of the portal to the destination bus to which the intercepted delay request message is addressed have been stored previously by step (c) in the register table recited in (a) (See Column 5 Lines 58-65); (f) synthesizing by the portal of a corresponding delay response message having the remote delay values for a remote transaction from the local bus of the portal to the destination bus where the intercepted delay request from step (e) is addressed by one of: (i) retrieving the remote delay values from the register table if said initial requester of the delay request message identified in step (e) is on the local bus of the portal; and (ii) calculating the remote delay values retrieved from the register table if said initial requester of the delay request message identified in step (e) is not on the local bus of the portal, wherein a max_remote_payload value is the smaller of max_remote payload values in one of: (1) the intercepted delay response message in step (b), and (2) the corresponding register table entry (See Column 5 Line 45 – Column 8 Line 34), and wherein remote timeout seconds, remote timeout cycles and hop count values in the intercepted delay request message are added to the corresponding register table entry to the destination bus,

respectively (See Column 5 Lines 33-44); and (g) sending the delay response message synthesized in step (f) to said initial requester of the delay request message intercepted in step (e) (See Column 5 Lines 61-65).

4. In reference to Claim 3, Suzuki teaches the limitations as applied to Claim 1 above. Suzuki further teaches that the source bus and destination bus comprise a serial bus connected by a bus bridge (See Column 4 Lines 31-35).

5. In reference to Claim 4, Suzuki teaches the limitations as applied to Claim 3 above. Suzuki further teaches that the source node and the destination node can communicate via a plurality of bus bridges, and thus an intermediate bus is inherently connected in a serial path between the source bus and the destination bus (See Column 2 Lines 35-37).

6. In reference to Claims 5 and 6, Suzuki teaches the limitations as applied to Claim 1 above. Suzuki further teaches that the source bus and destination bus are connected via a bridged network and that said bridged network comprises an IEEE 1394 bridged network (See Figure 1, Column 1 Lines 47-63, and Column 4 Lines 31-38).

7. In reference to Claim 7, Suzuki teaches (a) providing a source bus and a destination bus in a serial path having an intermediate bus connected between the source bus and destination bus via bridges (See Column 2 Lines 35-37 and Column 4

Lines 31-35); (b) intercepting by a portal of said intermediate bus a delay response message, which is equivalent to a timeout response message, sent from an exit portal of the destination bus to a particular delay requesting node on the source bus (See Column 4 Line 65 – Column 5 Line 10); (c) storing first remote delay values from the delay response message intercepted in step (b) in a storage area of said portal of said intermediate bus and forwarding the delay response message intercepted in step (b) to said particular delay requesting node on the source bus (See Column 4 Line 53 – Column 5 Line 44); (d) intercepting by said portal of said intermediate bus a subsequent delay request message from a subsequent requesting node of said plurality of nodes of said source bus to a node of said plurality of nodes of said destination bus (See Column 5 Lines 58-65); (e) said portal of the intermediate bus calculating a remote delay values from the source bus to the destination bus by adding the first delay values stored in step (c) to second remote delay values between the source bus and the intermediate bus except for a max_remote payload value (See Column 5 Line 45 – Column 8 Line 34); (f) synthesizing a delay response message by said portal of said intermediate bus, said synthesized delay response including the total delay values calculated in step (e) (See Column 5 Line 45 – Column 8 Line 34); and (g) forwarding said synthesized delay response message to said subsequent requesting node of said source bus in step (d) that initiated the delay request message (See Column 5 Lines 61-65).

8. In reference to Claim 8, Suzuki teaches the limitations as applied to Claim 7 above. Suzuki further teaches that the max_remote payload value is a smallest of max-

remote payload values in the values intercepted in the message and a corresponding register table entry to the destination bus (See Column 5 Line 45 – Column 8 Line 34).

9. In reference to Claim 9, Suzuki teaches the limitations as applied to Claim 8 above. Suzuki further teaches that the source bus, the intermediate bus, and the destination bus are connected by a bridged network (See Figure 1, Column 1 Lines 47-63, and Column 4 Lines 31-38).

10. In reference to Claim 11, Suzuki teaches the limitations as applied to Claim 7 above. Suzuki further teaches storing the delay values of the delay response message in a storage area of the source bus (See Figure 1 Numbers 112 and 300 and Column 5 Lines 11-44).

11. In reference to Claim 13, Suzuki teaches the limitations as applied to Claim 7 above. Suzuki further teaches that said source bus and said destination bus comprise a 1394 IEEE bridged network (See Figure 1, Column 1 Lines 47-63, and Column 4 Lines 31-38).

12. In reference to Claim 15, Suzuki teaches the limitations as applied to Claim 13 above. Suzuki further teaches that the source node and the destination node can communicate via a plurality of bus bridges, and thus the network inherently includes a

plurality of buses serial connected between the source bus and the destination bus (See Column 2 Lines 35-37).

13. In reference to Claim 16, Suzuki teaches a source bus having a first portal with a register table (See Figure 1 Numbers 102, 112, and 300 and Column 5 Lines 11-44); at least one intermediate bus having a bridge comprising a second portal including a register table (See Figure 1 Numbers 102, 112, and 300; Column 2 Lines 35-37; and Column 5 Lines 11-44); a destination bus having an exit portal (See Figure 1 Numbers 103, 106, and 107); a plurality of bus bridges which serially connects said source bus, said at least one intermediate bus and said destination bus (See Figure 1 Number 101 and Column 2 Lines 35-37); said first portal of the source bus including means for receiving a delay request, which is equivalent to a TIMEOUT request, from a node attached thereto (See Figure 1 and Column 5 Lines 58-65); said exit portal of said destination bus including means for receiving a delay request message and for sending a delay response message having delay values included therein (See Column 4 Line 65 – Column 5 Line 10); intercepting and storing means for intercepting by the bridge portal of said intermediate bus the delay response message sent by the exit portal of the destination bus, and for storing delay values of the delay response message from the exit portal of said destination bus in the register table of the bridge portal of the intermediate bus (See Figure 1 Numbers 112 and 300 and Column 4 Line 65 – Column 5 Line 44); means for intercepting and synthesizing, in which said second portal of said intermediate bus intercepts a delay request from a node on said source bus, and when

an ID of the destination bus in the delay request matches an ID of said destination bus having its delay values stored in the register table of the second portal of the intermediate bus, the second portal synthesizing a delay response message comprising a total delay values by adding the delay values between said destination bus and said intermediate bus and the delay values between said source bus and said intermediate bus, except for max_remote payload values, which is a smaller of the intercepted delay request message and corresponding table entry (See Column 5 Line 33 – Column 8 Line 34), means for transmitting the synthesized delay response message having the total delay values sent to the requesting node on said source bus (See Figure 1 Number 105 and Column 5 Lines 61-65).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki as applied to Claims 1, 7, 11, and 16 above, and further in view of The Free On-Line Dictionary of Computing ("FOLDOC").

16. In reference to Claim 2, Suzuki teaches the limitations as applied to Claim 1 above. Suzuki does not teach that the storage area for the register table comprises RAM. FOLDOC teaches the use of RAM as a common type of memory storage (See entry 'random-access memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Suzuki using random access memory, resulting in the invention of Claim 2, because RAM is a commonly used type of memory that allows for higher speed access because the order of access to different locations does not affect the speed of access (See entry 'random-access memory' in FOLDOC).

17. In reference to Claim 10, Suzuki teaches the limitations as applied to Claim 7 above. Suzuki further teaches that the storage area is a memory of a portal on said intermediate bus (See Figure 1 Numbers 112 and 300; Column 2 Lines 35-37; and Column 5 Lines 11-44). Suzuki does not teach that the storage area is a RAM of a portal on said intermediate bus. FOLDOC teaches the use of RAM as a common type of memory storage (See entry 'random-access memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Suzuki using random access memory, resulting in the invention of Claim 10, because RAM is a commonly used type of memory that allows for higher speed access because the order of access to different locations does not affect the speed of access (See entry 'random-access memory' in FOLDOC).

18. In reference to Claim 12, Suzuki teaches the limitations as applied to Claim 11 above. Suzuki does not teach that the storage area is a RAM of an entry portal. FOLDOC teaches the use of RAM as a common type of memory storage (See entry 'random-access memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Suzuki using random access memory, resulting in the invention of Claim 12, because RAM is a commonly used type of memory that allows for higher speed access because the order of access to different locations does not affect the speed of access (See entry 'random-access memory' in FOLDOC).

19. In reference to Claim 14, Suzuki and FOLDOC teach the limitations as applied to Claim 12 above. Suzuki further teaches that said source bus, said intermediate bus, and said destination bus comprise a 1394 IEEE bridged network (See Figure 1, Column 1 Lines 47-63, and Column 4 Lines 31-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Suzuki using random access memory, resulting in the invention of Claim 14, because RAM is a commonly used type of memory that allows for higher speed access because the order of access to different locations does not affect the speed of access (See entry 'random-access memory' in FOLDOC).

20. In reference to Claim 17, Suzuki teaches the limitations as applied to Claim 16 above. Suzuki does not teach that the means for storage comprises RAM. FOLDOC teaches the use of RAM as a common type of memory storage (See entry 'random-access memory').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Suzuki using random access memory, resulting in the invention of Claim 17, because RAM is a commonly used type of memory that allows for higher speed access because the order of access to different locations does not affect the speed of access (See entry 'random-access memory' in FOLDOC).

Claim Objections

21. Claim 7 is objected to because of the following informalities: In Item (d) Lines 1-2, the phrase "said intermediate bus" is repeated. Appropriate correction is required.

Drawings

22. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: Number 142 on Page 9 Lines 7, 15, and 19; and Page 10 Lines 2, 11, 13,

and 16. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

23. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1 Numbers 134 and 144. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

24. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "143" has been used to designate both "PORTAL" in Figure 1 and "internal register table entry" on Page 8 Lines 11-12; Page 15 Lines 17-18; and Page 16 Lines 7-8. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 6,548,559 to Pfister et al. ("Pfister") teaches determining timeout values for all switches that participate in the routing of a request. US Patent Application Publication Number 2002/0057655 to Staats ("Staats") teaches determining the speed between a first and second node on an IEEE-1394 bus by computing the speed between the first node and an intermediate node and computing the speed between the intermediate node and the second node. US Patent Application Publication Number 2004/0044801 to Haupt et al. ("Haupt") teaches determining a timeout delay in a network having multiple bridges.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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